Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a plurality of arrays activated independently from each other;

a plurality of burst read circuits provided in correspondence to the plurality of arrays, each burst read circuit successively reading a plurality of bits of data from a corresponding array; and

a burst interrupt circuit for activating a first burst read circuit while a second burst read circuit is activated.

[c2] 2. The semiconductor storage device according to Claim 1, further comprising:

a plurality of burst write circuits provided in correspondence to the plurality of arrays, each burst write circuit successively writing a plurality of bits of data in a corresponding array; and

a burst interrupt circuit for activating a first burst write circuit while a second burst write circuit is activated.

[c3] 3. A semiconductor storage device comprising:

a plurality of segment arrays, each including a plurality of unit arrays;

a plurality of segment selector circuits provided in correspondence to the plurality of segment arrays, each segment selector circuit activating a corresponding segment array;

a plurality of unit array selector circuits provided in correspondence to the plurality of segment arrays, each unit array selector circuit selectively activating the plurality of unit arrays included in a corresponding segment array;

a plurality of burst read circuits provided in correspondence to the plurality of segment arrays, each burst read circuit successively reading a plurality of bits of data from a unit array activated by the unit array selector circuit from among the plurality of unit arrays included in a corresponding segment array; and

a burst interrupt circuit for activating a first burst read circuit while a second burst read circuit is activated.

[c4] 4. The semiconductor storage device according to Claim 3, wherein

each of the burst read circuits includes a first prefetch latch circuit that is activated in response to a first read enable signal, and latches a plurality of bits of data read from a unit array activated by the unit array selector circuit; and

the burst interrupt circuit activates the first read enable signal for the first prefetch latch circuit that corresponds

to a segment array activated by the segment selector circuit.

[c5] 5. The semiconductor storage device according to Claim 4, wherein each of the burst read circuits further comprises:
a second prefetch latch circuit activated in response to a second read enable signal to latch a plurality of bits of data read from another unit array activated by the unit array selector circuit; and
the burst interrupt circuit activates the second read enable signal for the second prefetch latch circuit that corresponds to a segment array activated by the segment selector circuit.

[c6] 6. The semiconductor storage device according to Claim 3, further comprising:
a plurality of burst write circuits provided in correspondence to the plurality of segment arrays, each successively writing a plurality of bits of data in its corresponding segment array.

[c7] 7. The semiconductor storage device according to Claim 6, wherein each of the burst write circuits includes a first preload latch circuit activated in response to a first write enable signal so as to latch a plurality of bits of data to be written to a first unit array activated by the unit array

selector circuit, and
the burst interrupt circuit activates the first write enable signal for the first preload latch circuit corresponding to a segment array activated by the segment selector circuit.

[c8] 8. The semiconductor storage device according to Claim 7, wherein
each of the burst write circuits further includes a masking device for partly masking a plurality of bits of data latched in the first preload latch circuit.

[c9] 9. The semiconductor storage device according to Claim 8, wherein
each of the burst write circuits further includes a second preload latch circuit activated in response to a second write enable signal to latch a plurality of bits of data to be written to a second unit array activated by the unit array selector circuit, and
the burst interrupt circuit activates the second write enable signal for the second preload latch circuit corresponding to a segment array activated by the segment selector circuit.